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GENERAL

Objective

To lead and support semiconductor modeling and simulation in the design of high-speed circuits to meet signal integrity (SI), power integrity (PI), and EMI-EMC regulatory requirements.

Summary

Electronics Engineer with extensive experience and education in SI, PI, EMI, and semiconductor modeling. Received multiple management awards for key SI contributions to the bottom line.

Co-authored *Semiconductor Modeling: For Simulating Signal, Power, and ElectroMagnetic Integrity*, Springer. October 2006. ISBN: 0-387-24159-0

Computer Skills

Cadence PCB, Model Integrity, Signal Integrity, Sonnet, SPICE, EMI simulator, RF, Saber system simulator, MAST modeling language, CAE, RAMCAD.

EMPLOYMENT HISTORY

Hamilton-Sundstrand, Rockford, IL Contract EMI-EMC Engineer, 2007-Present

Working on the Boeing 787 project, doing EMI-EMC, testing, trouble-shooting, modeling, simulation, test procedures and debug. Lightning, radiated and conducted emissions, and susceptibility on microprocessor controlled aircraft power distribution system in an anechoic chamber to meet regulatory requirements per DO-160E.

Leventhal Design & Communications, Arlington Heights, IL

Consultant, speaker, and author in the areas of SI, PI, EMI-EMC, and IBIS modeling.

- **Cinch Connectors, Downers Grove, IL** Consultant, Connector Modeling Engineer, 2006–2007
S-Parameter model extraction and connector and flex board design to 18 GHz and beyond with CST Microwave Suites tools.
- **Johnson Controls Automotive, Holland, MI** Consultant, IBIS Modeling Engineer, 2002
Provided modeling support and consultation for EMI simulator company clients. Installed software, brought in Allegro board files, created IBIS library, trained client, and helped clients pass regulatory requirements.
- **Northrop-Grumman, Rolling Meadows, IL** Consultant, Lead Signal Integrity Engineer, 2001
Provided modeling support and consultation for EMI simulator company clients. Installed software, brought in Allegro board files, created IBIS library, and trained client.
- **IEEE Chicago/Rockford Consulting Group and IEEE-EMC Society** Taught signal integrity and EMI-EMC at IEEE meetings.
- **IBIS Committee** Served as librarian for IBIS model sources. Active in model quality sub-committee.

CommWorks, Rolling Meadows, IL (3Com Carrier R&D), Lead Signal Integrity Engineer, 1998-2002

Simulate signal integrity (SI), crosstalk, ground bounce and EMI behavior on high-speed digital backplanes and telecommunications boards. Provide expert advice and problem solving on layout, termination, routing, timing and other SI issues. Provided SI support for large and complex server boards using advance technology ICs. Typically did whole board scans, statistical, and worst case analysis. Constraints, topology and timing rules developed and driven into layout and routing. Clock speeds commonly 100 MHz and often much higher. Data speeds into the GBITS. Develop and deliver training seminars/labs to engineers and PCB designers. Started at average of 3.5 and progressed to 1.1 for first working prototype. Provide IBIS support and model verification on over 800 ICs. Correct model problems. Develop ISO9000 documentation and processes.

Cadence Design Systems, Chelmsford, MA Lead SI Applications Customer Support Engineer, 1996-1998

Provided expert help to FAEs and customers on the hotline for high-speed digital PCB design tools. Evaluate the signal integrity simulator and the models used. Plan, develop and deliver curriculum and courses for FAEs. Download and test the latest software before its release and work to correct and enhance it with the code developers. Prepare and release Knowledge Database solutions through the company website.

Motorola Automotive (AIEG), Northbrook, IL Consultant Lead Analog Simulation Engineer, 1994-1995

Integrated Mentor and SABER EDA tools. Provided analog SPICE, PSPICE, and SABER simulation and problem solving.

GE Medical Systems (ESI Group), Waukesha, Wisconsin 1983-1994

- **Computer Aided Project Engineer**

Provided CAE support engineering for X-RAY, CATSCAN, Magnetic Resonance, Ultrasound, and PETSCAN. Integrated Mentor-(V7) and Saber (V3.2). Developed GUI for users. Beta site tested Analog's FRAMEWAY Library and symbol integrated one year ahead of schedule. Evaluated software tools for thermal, MTBF, reliability, RF, and EMC analysis. Developed strategies for new CAE tools.

- **Component Engineering Project Manager**

Initiated and developed IBM mainframe component database containing over 48,000 electrical and mechanical components. Supervised 5 subordinates and coordinated inputs from 3 programmers, 51 designers, and consultants. Negotiated for programming support, tested software, and gave final approval. Designed user-friendly GUI. Database saves \$3M per year. Won GE Management Award for paperless drawing system. Developed selection guide of 600 transistors covering the range of application as 27,000 transistors available in market. Led component standardization, alternate source part substitution and phase-out of obsolete items. Participated with 6 cross-functional teams (35 people) mapping the engineering design and development process. A complete set of process maps and improvement principles was produced. Authored the top-level ISO-9000 quality manual and participated on the team that developed the ISO-9000 Engineering Quality Manual.

EMPLOYMENT HISTORY PRIOR TO 1983

Includes: Semiconductor modeling and applications engineering; Device physics, failure analysis, and semiconductor process engineering; Reliability and quality engineering; Component engineering, and; RF circuit and amplifier design engineering.

EDUCATION

MSEE Illinois Institute of Technology, Chicago, Illinois.

Additional Post-Graduate work completed, including semiconductor device physics, RF and microwave engineering at the University of Santa Clara and University of Wisconsin - Milwaukee.

Other training: A list of many other courses taken is available on request.

Other publications: Numerous other publications on engineering subjects are available on request.